IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| In re Application of: Luiz Andre Barroso et al. | § | Group Art Unit: | 2186 |
| Serial No.: 10/693,388 | § | Examiner: | Unassigned |
| Filed: October 24, 2003 | § | | |
| For: SCALABLE ARCHITECTURE BASED ON SINGLE-CHIP MULTIPROCESSING | § | Atty. Docket: | **200301825-5** |

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

CERTIFICATE OF MAILING
37 C.F.R. 1.8

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date below:

March 8, 2004 — Helen Tinsley
Date — Helen Tinsley

Sir:

**EXPLANATION REGARDING SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**
**PURSUANT TO 37 C.F.R. § 1.97(b)**

In compliance with the duty of disclosure under 37 C.F.R. § 1.56(a), it is respectfully requested that this Supplemental Information Disclosure Statement be entered and that the listed references be considered by the Examiner and made of record. The Applicant is resubmitting the references listed under "Other References" because only the first pages of those references were available to the Applicant at the time of filing the original Information Disclosure Statement. Since that time, the Applicant has obtained the remaining pages of the references.

In accordance with 37 C.F.R. § 1.97, this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made, as an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R.

§1.56(b), or as a representation that no other possibly material information, as defined in 37 C.F.R. § 1.56(b), exists.

Furthermore, the references listed on the attached Form 1449 are not to be construed as an admission that these references qualify as prior art as to the above-referenced application or any related application. Rather, these references are being presented for the Examiner's consideration without prejudice to the right to demonstrate that any of these references do not qualify as prior art should the Examiner choose to apply any of these references.

Respectfully submitted,

Date: March 8, 2004

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PATENT APPLICATION

ATTORNEY DOCKET NO. 200301825-5

**IN THE**
**UNITED STATES PATENT AND TRADEMARK OFFICE**

**Inventor(s):** Luiz Andre Barroso et al. **Confirmation No.:**

**Application No.:** 10/693,388 **Examiner:**

**Filing Date:** 10-24-2003 **Group Art Unit:** 2186

**Title:** SCALABLE ARCHITECTURE BASED ON SINGLE-CHIP MULTIPROCESSING

**Commissioner for Patents**
**PO Box 1450**
**Alexandria, VA 22313-1450**

~~SUPPLEMENTAL~~ INFORMATION DISCLOSURE STATEMENT

**Sir:**

This Information Disclosure Statement is submitted:

(X) under 37 CFR 1.97(b), or
(Within three months of filing national application; or date of entry of national application; or before mailing date of first office action on the merits; whichever occurs last)

( ) under 37 CFR 1.97 (c) together with either a:
( ) Statement under 37 CFR 1.97(e), or
( ) a $180.00 fee under 37 CFR 1.17(p), or
(After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first)

( ) under 37 CFR 1.97 (d) together with a:
( ) Statement under 37 CFR 1.97(e)(1) or (2), and
( ) a $180.00 fee set forth in 37 CFR 1.17(p).
(Filed after final action, a notice of allowance, on or before payment of the issue fee)

Please charge to Deposit Account **08-2025** the sum of $0.00 . At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **08-2025** pursuant to 37 CFR 1.25.

(X) Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Statement together with any required copies of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

( ) A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individuals(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

It is requested that the information disclosed herein be made of record in this application.

(X) I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450. Date of Deposit: 03-08-2004

OR

( ) I hereby certify that this paper is being transmitted to the Patent and Trademark Office facsimile number _____ on _____
Number of pages:

Typed Name: Helen Tinsley
Signature: Helen Tinsley

Respectfully submitted,

**Luiz Andre Barroso et al.**

By Barry D. Blount

**Barry D. Blount**
Attorney/Agent for Applicant(s)
Reg. No. **35,069**

Date: **03-08-2004**

Telephone No.: **(281) 970-4545**

FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

| ATTY. DOCKET NO. | APPLICATION NO. | CONFIRMATION NO. |
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| 200301825-5 | 10/693,388 | |
| APPLICANT: Luiz Andre Barroso et al. | | |
| FILING DATE: 10-24-2003 | GROUP: 2186 | |

**REFERENCE DESIGNATION** **U.S. PATENT DOCUMENTS**

| EXAMINER INITIAL | | DOCUMENT NUMBER | PUBLICATION DATE | NAME | Pages, Columns, Lines Where Relevant Passages or Figures Appear |
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| | 1B | 5,778,437 | 07-07-98 | Baylor et al. | |
| | 1C | 6,295,598 | 09-25-01 | Beroni et al. | |
| | 1D | 6,202,127 | 03-13-01 | Dean et al. | |
| | 1E | 5,457,679 | 10-10-95 | Eng et al. | |
| | 1F | 5,440,752 | 08-08-95 | Lentz et al. | |
| | 1G | 6,457,100 | 09-24-02 | Ignatowski et al. | |
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**OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)**

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| | 1Q | Agrawal, Anant, et al., "An Evaluation of Directory Schemes for Cache Coherence", Proceedings of 15th International Symposium on Computer Architecture ("ISCA") (May 1998) pp. 280-289 |
| | 1R | Barroso, Luiz Andre, et al., "Impact of Chip-Level Integration on Performance of OLTP Workloads", High-Performance Computer Architecture ("HPCA") (January 2000) |
| | 1S | Barroso, Luiz Andre, et al., "Memory System Characterization of Commercial Workloads", ISCA (June 1998) |

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| | 2Q | Eggers, Susan J., et al., "Simulation Multithreading: A Platform for Next-generation Processors", University of Washington, DEC Western Research Laboratory ((eggers.levyjlo)@cs.washington.edu) ((emer.stamm)@vssad.enet.dec.com) pp. 1-15 |
| | 2R | Eickemeyer, Richard J., et al., "Evaluation of Multithreaded Uniprocessors for Commercial Application Environments", ACM (1996) (0-89791-786-3) pp. 203-213 |
| | 2S | Gupta, Anoop, et al., "Reducing Memory and Traffic Requirements for Scalable Directory-Based Cache Coherence Schemes", Stanford University, Computer Systems Laboratory, pp 1-10 |

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| | 3Q | Hammond, Lance, et al., "A Single-Chip Multiprocessor", IEEE (September 1997) (0018-9162) |
| | 3R | Hammond, Lance, et al., "Data Speculation Support for a Chip Multiprocessor", Stanford University, Computer Systems Laboratory (http://www.hydra.stanford.edu/) |
| | 3S | Jouppi, Norman P., et al., "Tradeoffs in Two-Level On-Chip Caching", WRL Research Report 93/3, Western Research Laboratory (WRL-Techreports@decwri.dec.com) (December 1993) pp. 1-31 |

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| | 4R | Kuskin, Jeffrey, et al., "The Stanford FLASH Multiprocessor", Stanford University, Computer Systems Laboratory |
| | 4S | Laudon, James, et al., "The SGI Origin: A ccNUMA Highly Scalable Server", Silicon Graphics, Inc. (laudon@sgi.com) |

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| | 5S | Nowatzyk, Andreas G., et al., "S-Connect: from Networks of Workstations to Supercomputer Performance", 22nd Annual International Symposium on Computer Architecture ("ISCA") (June 1995) |

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| | 6Q | Nowatzyk, Andreas, et al., "Exploiting Parallelism in Cache Coherency Protocol Engines", Sun Microsystems Computer Corporation |
| | 6R | Olukotun, Kunle, et al., "The Case of a Single-Chip Multiprocessor", Proceedings Seventh International Symposium Architectural Support for Programming Languages and Operating Systems ("ASPLOS VII") (October 1996) |
| | 6S | Steffan, J. Gregory, et al., "The Potential for Using Thread-Level Data Speculation to Facilitate Automatic Parallelization", HPCA-4 (February 1998) pp. 1-12 |

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| | 7Q | Tremblay, Marc, "MAJC-TM-5200 AVLIW Convergent MPSOC", Sun Microsystems, Inc., Microprocessor Forum (1999) |
| | 7R | Kunkel, Steven, et al., "System Optimization for OLTP Workloads, IEEE (1999) (0272-1732) pp. 56-64 |
| | 7S | Diefendorff, Keith, "Power4 Focuses on Memory Bandwidth", Microdesign Resources, Microprocessor Report vol 13 No. 13, October 6, 1999 |

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| | 8Q | Hammond, Lance, et al., "The Stanford Hydra CMP", Stanford University, Computer Systems Laboratory (http://www-hydra.stanford.edu) |
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